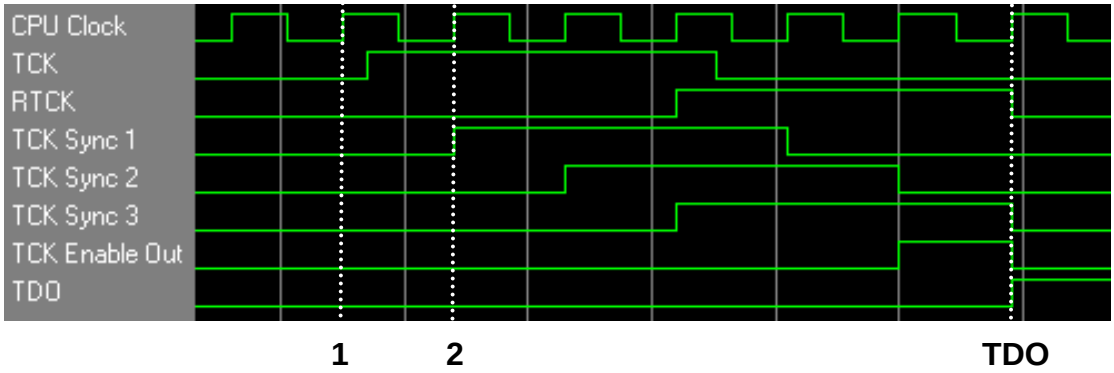
Turbo TCK Synchronizer
for synthesizable ARM cores

This document describes the new high performance TCK synchronizer from Debug Innovations. A TCK synchronizer is required to interface synthesizable ARM cores to standard JTAG compliant products such as ICEs and production test equipment.

The standard ARM design has a significant effect on debug performance at low to medium CPU clock speeds. This paper explains why this is the case and introduces an alternative design with three times the performance of the standard ARM design.

The standard ARM TCK synchronizer circuit.

ARM publish a standard TCK synchronizer circuit for use with –S devices (synthesizable ARM cores). The timing for this circuit is shown below:



A transaction is initiated by the ICE on the rising edge of TCK at an unspecified point between two rising edges of the CPU clock (points 1 and 2 above). Two flip-flops are used to synchronize TCK to the CPU clock (TCK Sync 1 and TCK Sync 2 signals) then a 3rd flip-flop is used to generate RTCK and TCK Enable. The rising edge of RTCK indicates to the ICE that it can issue the falling edge of TCK, then the falling edge propagates through the 2 flip-flops until RTCK goes low. At this point (TDO above) TDO is available and typically will be read by the ICE on the next rising edge of TCK (or after a similar delay if there are no more pending TCKs).

In the best case, the total TCK transaction time is 5 CPU clocks (from point 2 to TDO). In the worst case, the total TCK transaction time is 6 CPU clocks (from point 1 to TDO). Therefore the average transaction time using the standard ARM synchronizer circuit is 5.5 clocks.

The time between the end of this TCK and the start of the next is dependant on the ICE and the CPU clock frequency. At low CPU clock frequencies the ICE will be able to issue a new TCK before the next CPU clock edge, effectively locking the ICE to the CPU clock. Hence, below a certain CPU clock frequency the performance of the ICE will become irrelevant and the synchronizer delay will completely determine the overall system debug performance. One TCK will be processed every 6 CPU clocks and the debug performance will be one sixth of the performance of an equivalent non-synthesizable ARM.

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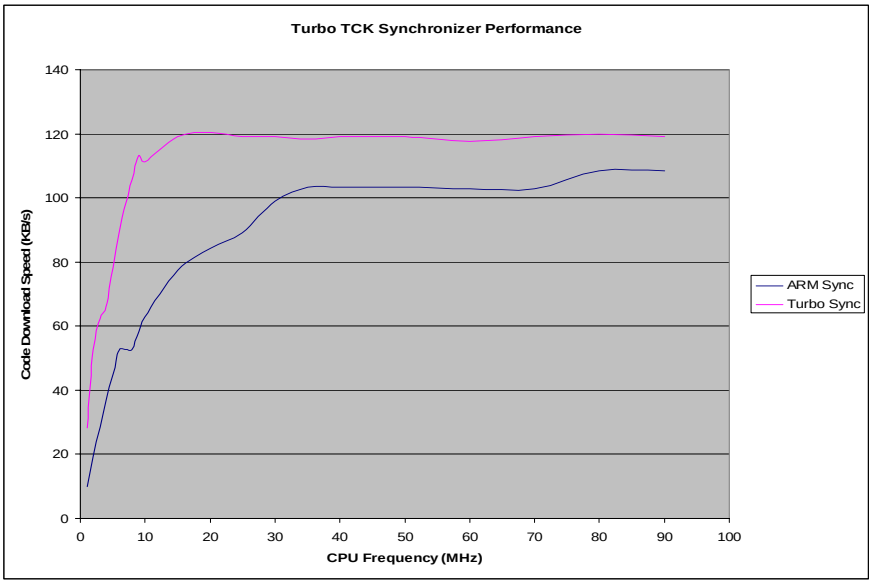
Unfortunately this is exactly when the performance is needed as most users download their code just after reset when the CPU's PLL is in bypass mode. Also the performance of modern ICEs is such that the synchronizer continues to have a noticeable effect at relatively high frequencies (up to around 100MHz). ARM based microcontrollers are particularly badly affected as they tend to have an upper clock frequency of around 40-60MHz. For example the Philips LPC2100 series based on the ARM7TDMI-S core typically starts up with a 10MHz CPU clock and has a maximum clock frequency of 60MHz. Therefore it is always operating in the region where the TCK synchronizer limits the debug performance.

Debug Innovations Turbo TCK synchronizer.

The Turbo TCK Synchronizer from Debug Innovations is a replacement for the standard ARM design. It provides all the same signals to the core and the ICE except it requires only 2 CPU clocks per TCK transaction resulting in a 3x improvement in JTAG performance. The advantages are:

1. Improved debug performance (particularly when downloading code).
2. Improved production test performance (test times will be reduced by a factor of 3).

The Turbo TCK Synchronizer also presents RTCK to the ICE earlier than the standard ARM design resulting in improved ICE performance. The graph below shows actual measured code download performance using ARM standard development tools (ADS and Multi-ICE).



At low CPU clock frequencies, the performance of the Turbo TCK Synchronizer is 3 times that of ARM's standard circuit, at 10MHz the performance is double and above 15MHz the full speed of the ICE is reached (faster ICEs and test equipment would take further advantage of the Turbo Synchronizer's performance) whereas ARM's standard synchronizer doesn't achieve full performance even at 90MHz.

The gate count and power consumption are similar to the standard ARM design and there are no extra resets or clocks required. Delivery is soft IP (VHDL).

Contact sales@debuginnovations.com for more details.