XOSC1
25.175MHz

OUTPUT 8 PIXCLK

25.175MHz Pixel Clock

U1
74AC163
VCC
nRST799
nSLEEP
PIXCLK
RST
PE
CET
CEP
CLK
P0
P1
P2
P3
GND
VCC
TC
Q0
Q1
Q2
Q3
HTC1
HA0
HA1
HA2
HA3

U2
74AC163
HTC2
HA4
HA5
HA6
HA7

U3
74AC163
HA8
HA9

U6
74HC4040
RST
VDD
CLK
QA
QB
QC
QD
QE
QF
QG
QH
QI
QJ
QK
QL
HSYNC
VA0
VA1
VA2
VA3
VA4
VA5
VA6
VA7
VA8
VA9

Vertical Address (Line) Counter

Horizontal Address (Pixel) Counter

U4A
74AC10
nHSYNC95

U4C
74AC10

U5A
74AC08

U4B
74AC10
nRST799

U5B
74AC08

U7A
74HC11
RST525
RST524

U8A
74HC74
D
PR
Q
CLR

U8B
74HC74
VSYNC

Vertical Sync Pulse Generation

U9A
74HC74
HSYNC
PIXCLK

Horizontal Sync Pulse Generation

Unused Flip-Flop

U9B
74HC74

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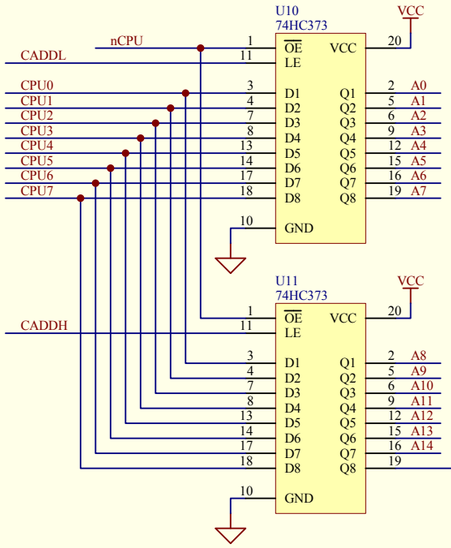
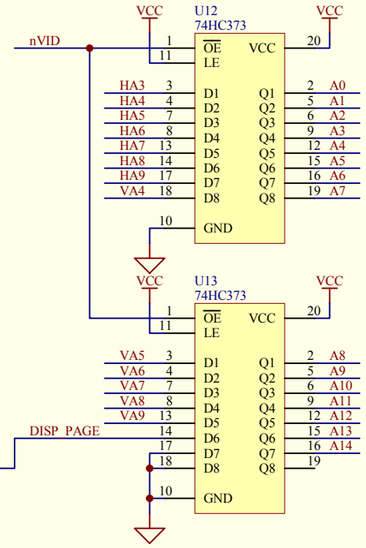
Title: TTL Terminal, H/V count & sync signals		
Size: A4	Number:	Revision: V1.1
Date: 10-Feb-2020	Sheet of	
File: C:\PCBs\VGA_Display\VGA_Terminal_V1.ddb	Drawn By:	

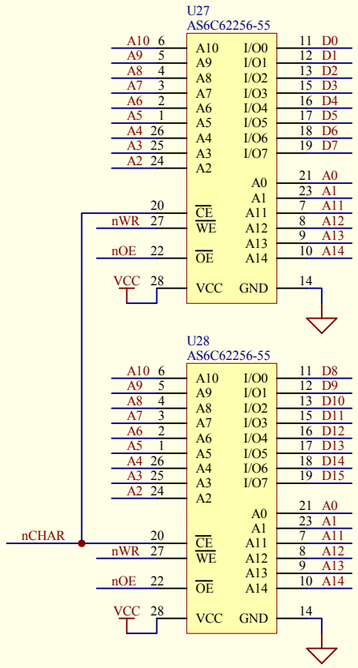
CPU Address Buffers



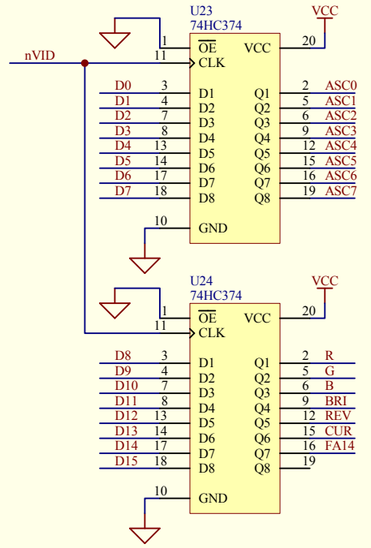
Video Address Buffers



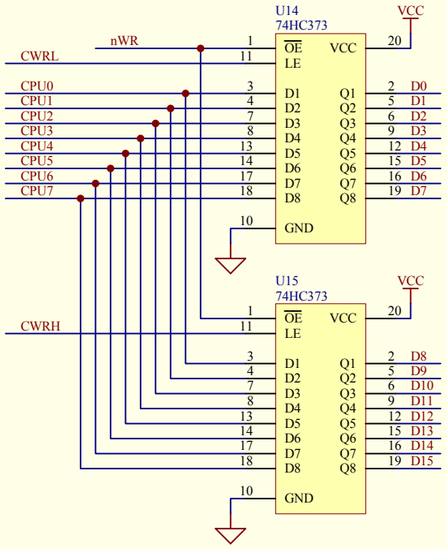
Character RAMs



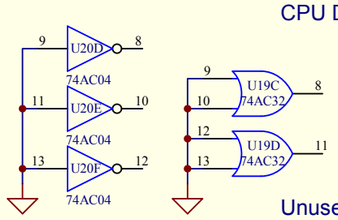
Video Data Read Buffers



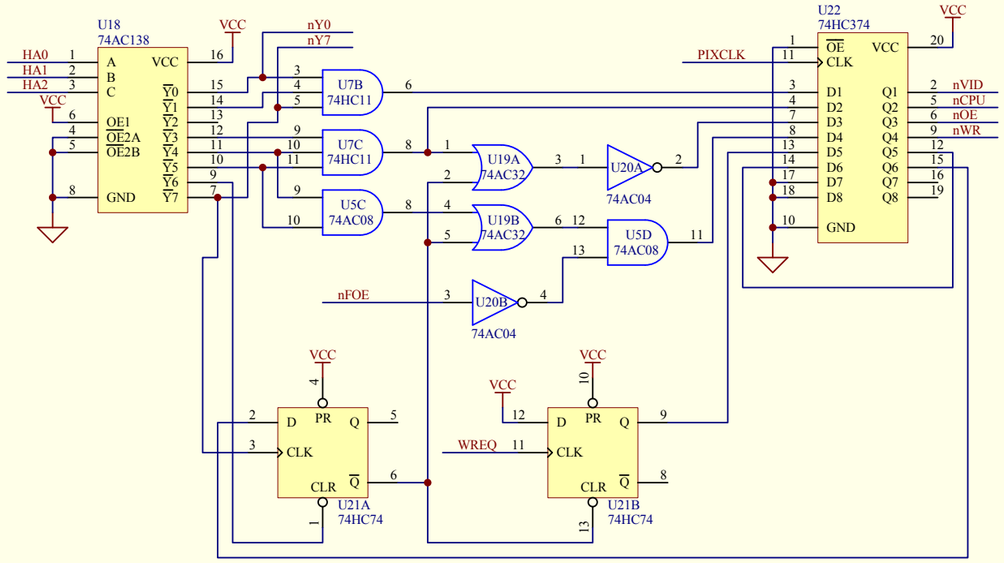
CPU Data Write Buffers



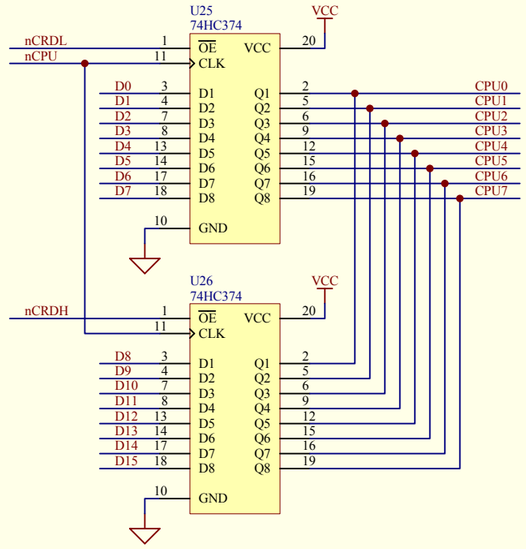
Unused gates



RAM Timing Generation



CPU Data Read Buffers



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Title: TTL Terminal, Character RAMs

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Pixel Shift Reg

Font RAM

U29
AS6C62256-55

ASC6 6 A10 I/O0 11 FD0
ASC5 5 A9 I/O1 12 FD1
ASC4 4 A8 I/O2 13 FD2
ASC3 3 A7 I/O3 15 FD3
ASC2 2 A6 I/O4 16 FD4
ASC1 1 A5 I/O5 17 FD5
ASC0 26 A4 I/O6 18 FD6
FA3 25 A3 I/O7 19 FD7
FA2 24 A2
A0 21 FA0
A1 23 FA1
20 CE A11 7 ASC7
nFWR 27 WE A12 8 REV
A13 9 CUR
nFOE 22 OE A14 10 FA14
VCC 28 VCC GND 14

U30
74HC165

nY0 1 S/L VCC 16
15 CLK INH
PIXCLK 2 CLK
10 SI
11 A
12 B
13 C QH 9 PIXELS
14 D
3 E
4 F QH 7
5 G
6 H
8 GND

U31
74HC175

1 CLR VCC 16
nY7 9 CLK
R 4 D1 Q1 2
Q1 3
G 5 D2 Q2 7
Q2 6
B 12 D3 Q3 10
Q3 11
BRI 13 D4 Q4 15
Q4 14
8 GND

U33A 74AC08 (1, 2 → 3)
U33B 74AC08 (4, 5 → 6)
U33C 74AC08 (9, 10 → 8)
U33D 74AC08 (12, 13 → 11)

Colour Re-timing

U20C
74AC04

6 → 5

Font Address Mux

U16
74HC373

1 OE VCC 20
CFONTA 11 LE
CPU0 3 D1 Q1 2
CPU1 4 D2 Q2 5
CPU2 7 D3 Q3 6
CPU3 8 D4 Q4 9
CPU4 13 D5 Q5 12 nCHAR
CPU5 14 D6 Q6 15 nSLEEP
CPU6 17 D7 Q7 16 nFOE
CPU7 18 D8 Q8 19 nFWR
10 GND

U32
74HC157

15 OE VCC 16
A/B 1
VA0 2 1A 1Y 4 FA0
3
VA1 5 2A 2Y 7 FA1
6
VA2 11 3A 3Y 9 FA2
10
VA3 14 4A 4Y 12 FA3
13
8 GND

U17
74HC373

1 OE VCC 20
nFWR 11 LE
CFONTD
3 D1 Q1 2 FD0
4 D2 Q2 5 FD1
7 D3 Q3 6 FD2
8 D4 Q4 9 FD3
13 D5 Q5 12 FD4
14 D6 Q6 15 FD5
17 D7 Q7 16 FD6
18 D8 Q8 19 FD7
10 GND

CPU Font Address & Data Buffers

R5 820R
R8 2K2
Q1 2N3904
R11 240R
R14 75R

R6 820R
R9 2K2
Q2 2N3904
R12 240R
R15 75R

R7 820R
R10 2K2
Q3 2N3904
R13 240R
R16 75R

R17 75R
R18 75R

RED
GREEN
BLUE
J4
VGA
6 1 11 7 2 12 8 3 13 9 4 14 10 5 15

HSYNC
VSYNC

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Title: TTL Terminal, Font RAM & Pixel Reg		
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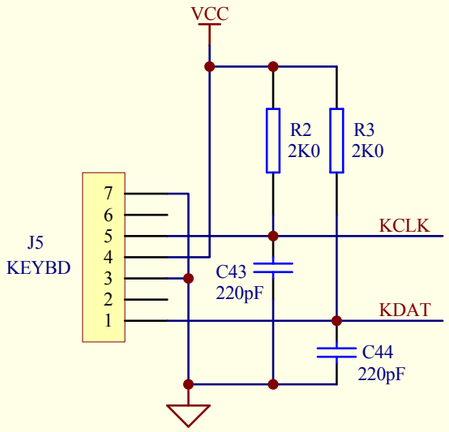
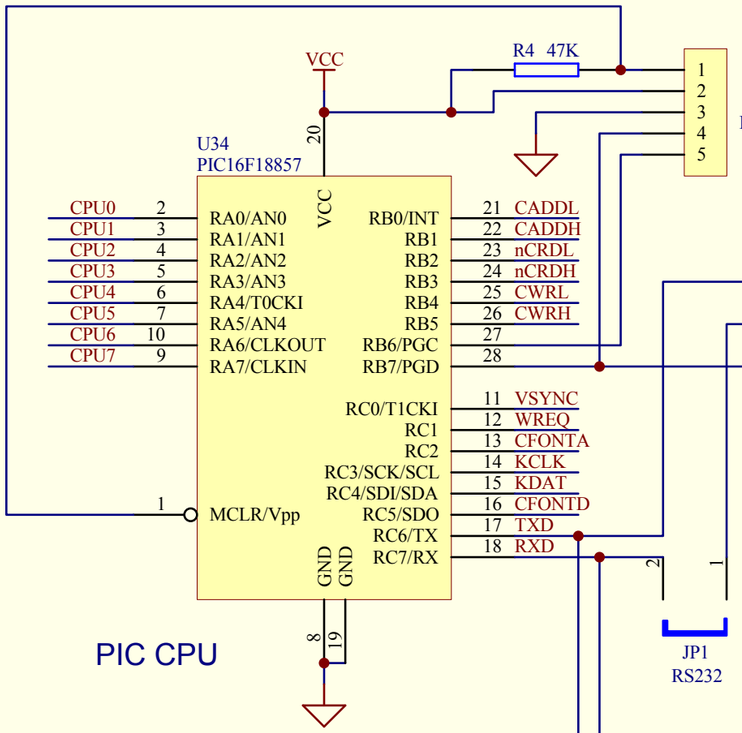
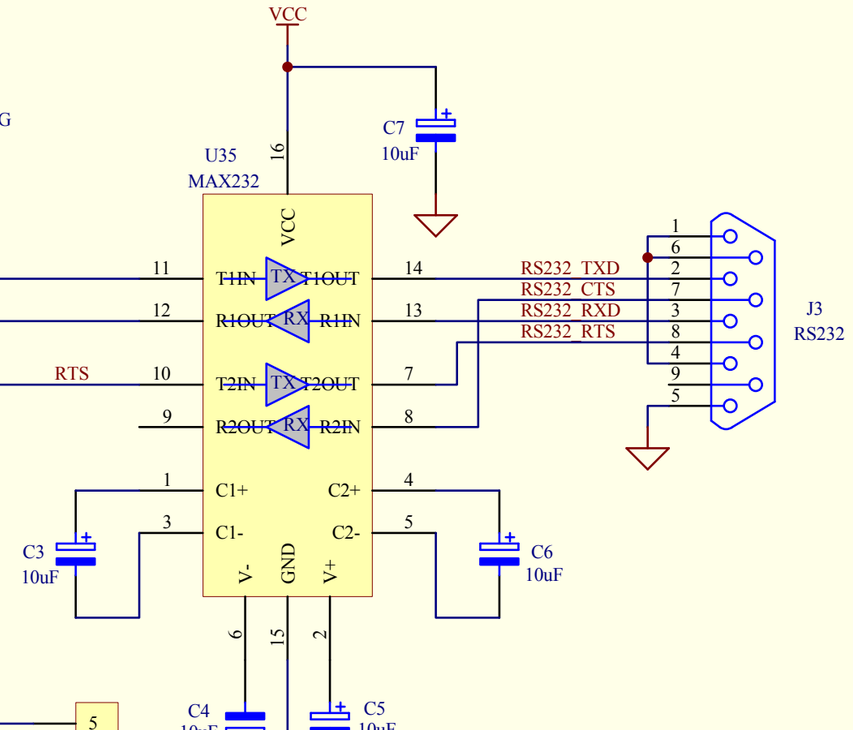
Keyboard



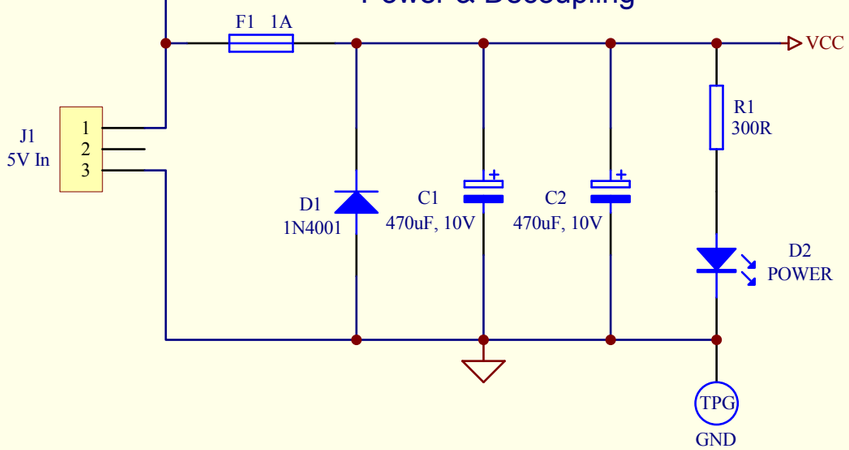
PIC CPU

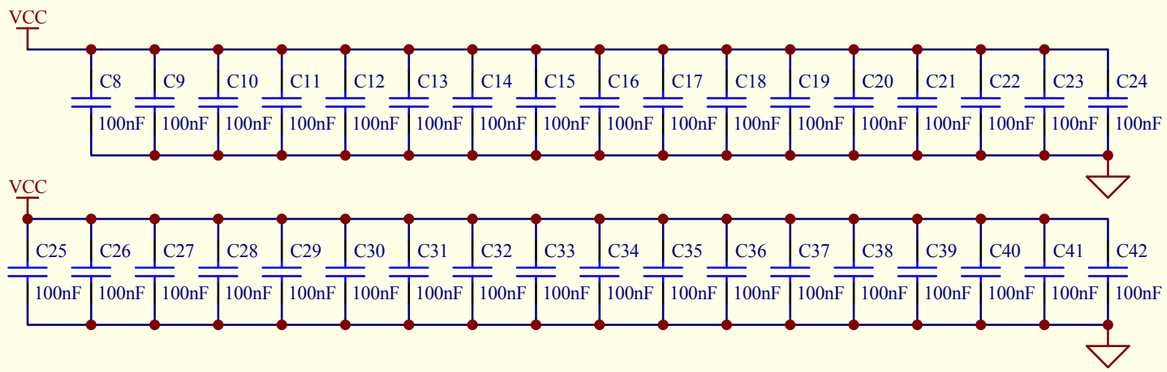


RS232 Driver



Power & Decoupling





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Title: TTL Terminal, CPU & Keyboard		
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Date: 10-Feb-2020	Sheet of	
File: C:\PCBs\VGA_Display\VGA_Terminal_V1.ddb	Drawn By:	