XOSC1
25.175MHz

OUTPUT 8 PIXCLK

25.175MHz Pixel Clock

U1
74AC163
VCC
nRST799
nSLEEP
PIXCLK
RST PE CET CEP CLK VCC TC P0 P1 P2 P3 Q0 Q1 Q2 Q3 GND
HTC1 HA0 HA1 HA2 HA3

U2
74AC163
HTC1
HTC2 HA4 HA5 HA6 HA7

U3
74AC163
HTC2
HA8 HA9

U6
74HC4040
RST VDD CLK QA QB QC QD QE QF QG QH QI QJ QK QL GND
HSYNC
VA0 VA1 VA2 VA3 VA4 VA5 VA6 VA7 VA8 VA9

U7A
74HC11

RST525
RST524

U8A
74HC74
D PR Q CLK CLR Q

Vertical Address (Line) Counter

U4A
74AC10
nHSYNC95

U4C
74AC10

U5A
74AC08

U4B
74AC10
nRST799

U5B
74AC08

U9A
74HC74
HSYNC
PIXCLK

U8B
74HC74
VSYNC

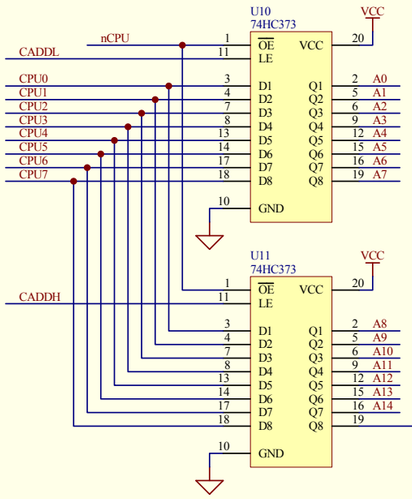
Vertical Sync Pulse Generation

Horizontal Sync Pulse Generation

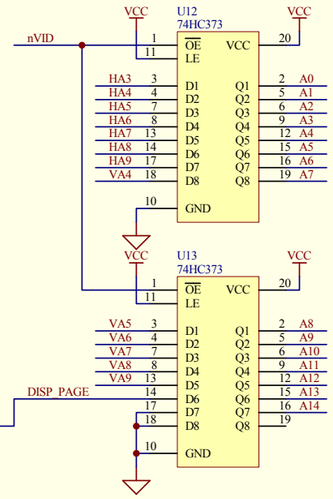
Horizontal Address (Pixel) Counter

Title: TTL Terminal, H/V count & sync signals		
Size: A4	Number:	Revision: V1.2
Date: 13-Mar-2023	Sheet of	
File: C:\PCBs\Computing\TTL_Terminal\TTL_Terminal_V1.2.ddb	Drawn By:	

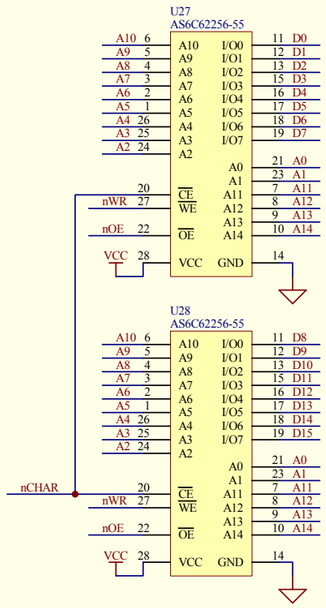
CPU Address Buffers



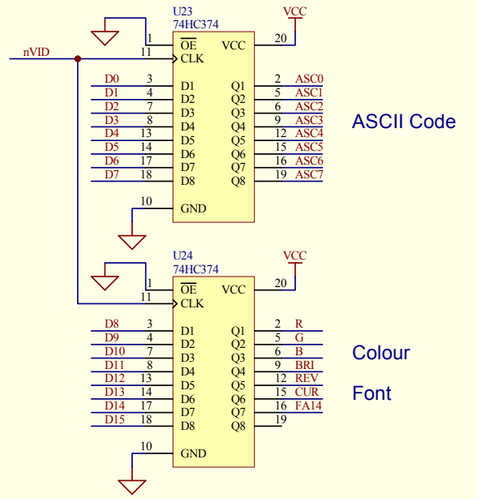
Video Address Buffers



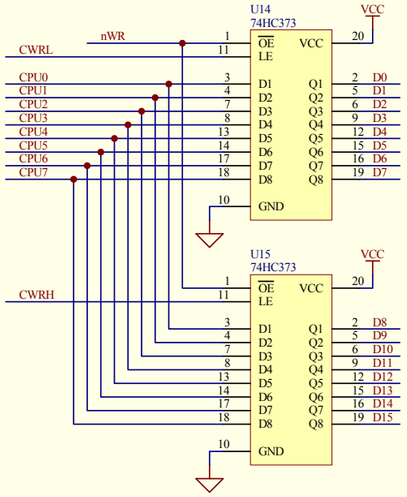
Character RAMs



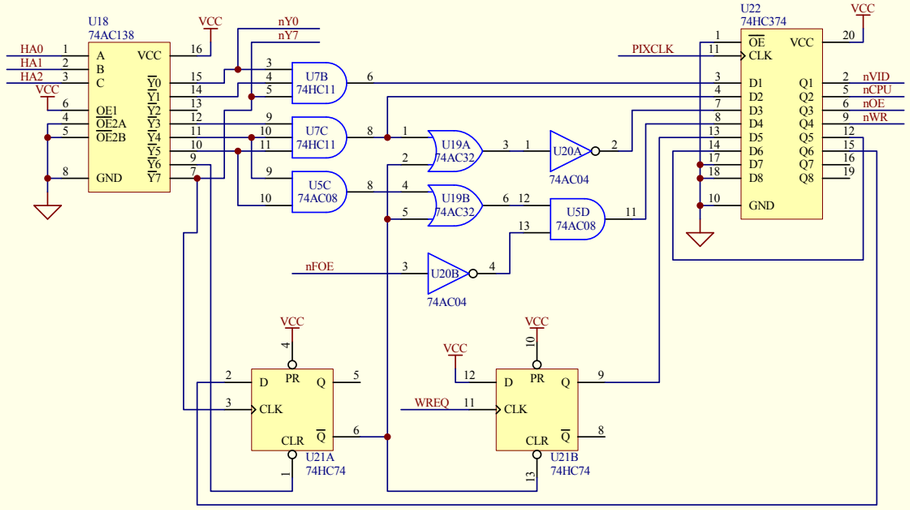
Video Data Read Buffers



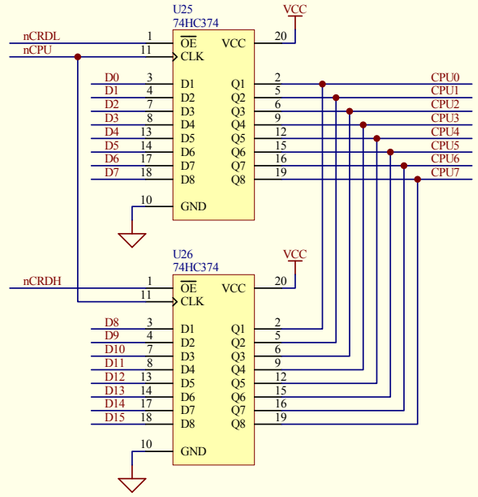
CPU Data Write Buffers



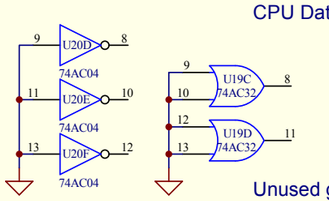
RAM Timing Generation



CPU Data Read Buffers



Unused gates



Title: TTL Terminal, Character RAMs

Size	Number	Revision
A3		V1.2

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Font RAM

U29
AS6C62256-55

ASC6 6
ASC5 5
ASC4 4
ASC3 3
ASC2 2
ASC1 1
ASC0 26
FA3 25
FA2 24

A10 A9 A8 A7 A6 A5 A4 A3 A2
I/O0 I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7
A0 A1 A11 A12 A13 A14
CE 20
WE nFWR 27
OE nFOE 22
VCC 28
GND 14

FD0 FD1 FD2 FD3 FD4 FD5 FD6 FD7
FA0 FA1 ASC7 REV CUR FA14

Pixel Shift Reg

U30
74HC165

nY0 1
PIXCLK 2
S/L 15
CLK INH 16
CLK 10
SI 11
A 12
B 13
C 14
D 3
E 4
F 5
G 6
H
QH 9 PIXELS
QH 7
GND 8
VCC 16

U31
74HC175

CLR 1
nY7 9
CLK
R 4
G 5
B 12
BRI 13
D1 D2 D3 D4
Q1 Q2 Q3 Q4
Q1 3
Q2 7
Q3 6
Q4 10
11
15
14
GND 8
VCC 16

Colour Re-timing

U20C
74AC04
6 5

U33A 74AC08 1 2 3
U33B 74AC08 4 5 6
U33C 74AC08 9 10 8
U33D 74AC08 12 13 11

RGB Drivers

R5 910R
R8 1K8
R11 470R
Q1 2N3904
R14 75R

R6 910R
R9 1K8
R12 470R
Q2 2N3904
R15 75R

R7 910R
R10 1K8
R13 470R
Q3 2N3904
R16 75R

R17 75R
R18 75R

RED
GREEN
BLUE
HSYNC
VSYNC

J4
VGA
6 1 11 7 2 12 8 3 13 9 4 14 10 5 15

U16
74HC373

CFONTA 11
CPU0 3
CPU1 4
CPU2 7
CPU3 8
CPU4 13
CPU5 14
CPU6 17
CPU7 18
OE 1
LE 11
D1 D2 D3 D4 D5 D6 D7 D8
Q1 2
Q2 5
Q3 6
Q4 9
Q5 12 nCHAR
Q6 15 nSLEEP
Q7 16 nFOE
Q8 19 nFWR
GND 10
VCC 20

U32
74HC157

VA0 2
VA1 5
VA2 11
VA3 14
OE 15
A/B 1
1A 3
1B 6
2A 10
2B 13
3A
3B
4A
4B
1Y 4 FA0
2Y 7 FA1
3Y 9 FA2
4Y 12 FA3
GND 8
VCC 16

Font Address Mux

U17
74HC373

CFONTD 11
OE 1
LE 11
D1 D2 D3 D4 D5 D6 D7 D8
Q1 2 FD0
Q2 5 FD1
Q3 6 FD2
Q4 9 FD3
Q5 12 FD4
Q6 15 FD5
Q7 16 FD6
Q8 19 FD7
GND 10
VCC 20

Buzzer Drive

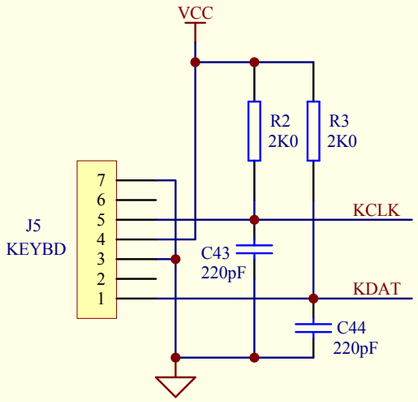
J7
Buzzer
1 2 3

U9B
74HC74
CWRH 11
D 12
PR 10
CLK
CLR 13
Q 9
Q 8
R19 1K2
Q4 2N3904

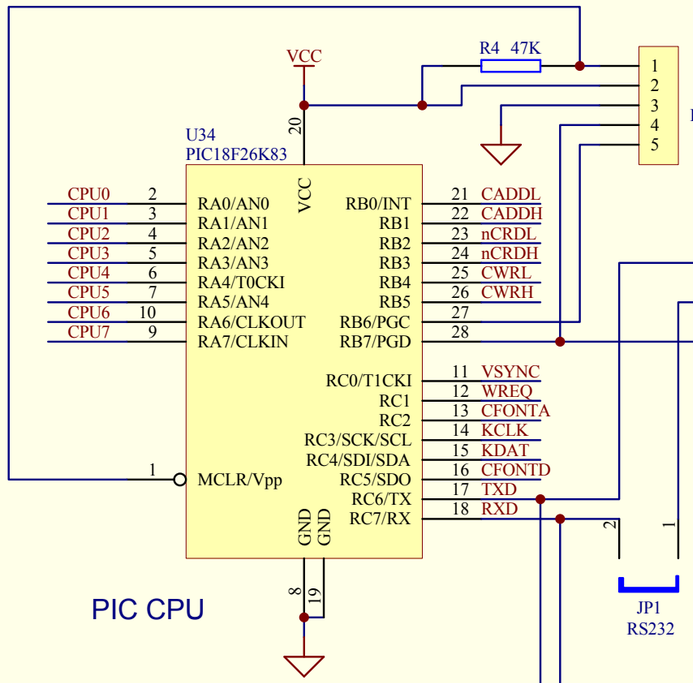
CPU Font Address & Data Buffers

Title	TTL Terminal, Font RAM & Pixel Reg	
Size A3	Number	Revision V1.2
Date: 13-Mar-2023		Sheet of
File: C:\PCBs\Computing\TTL_Terminal\TTL_Terminal_V1.2.ddb		Drawn By

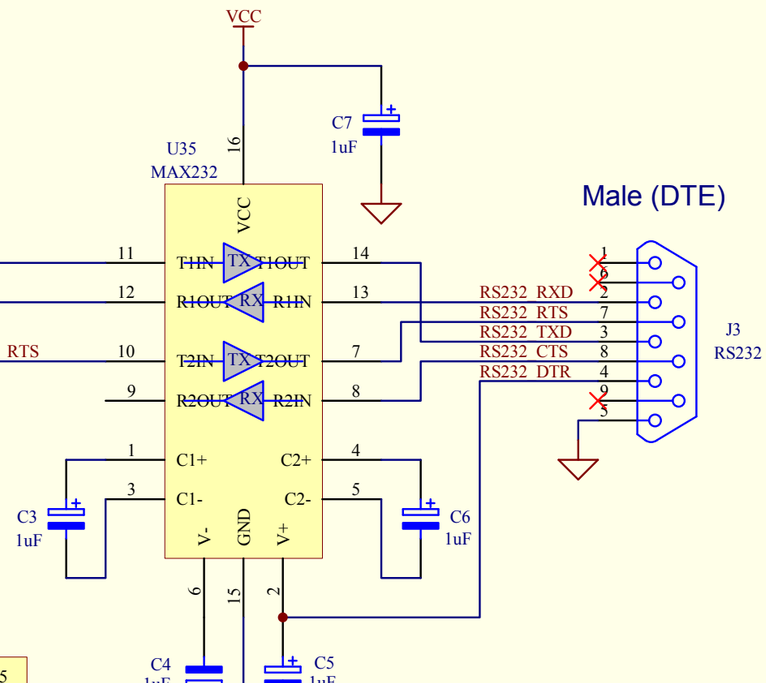
Keyboard



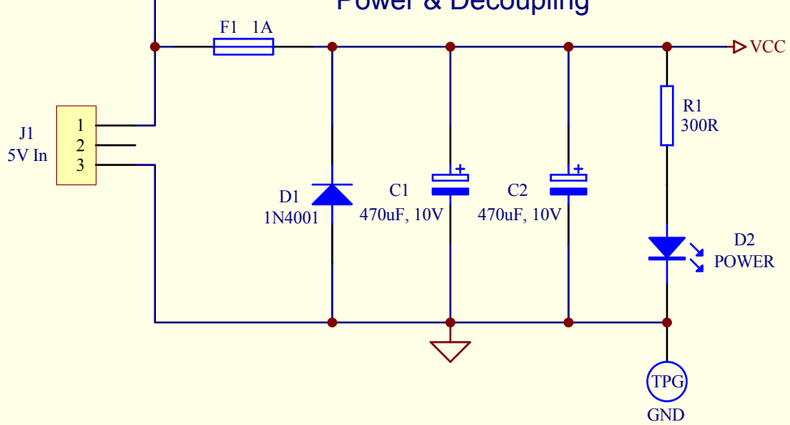
PIC CPU

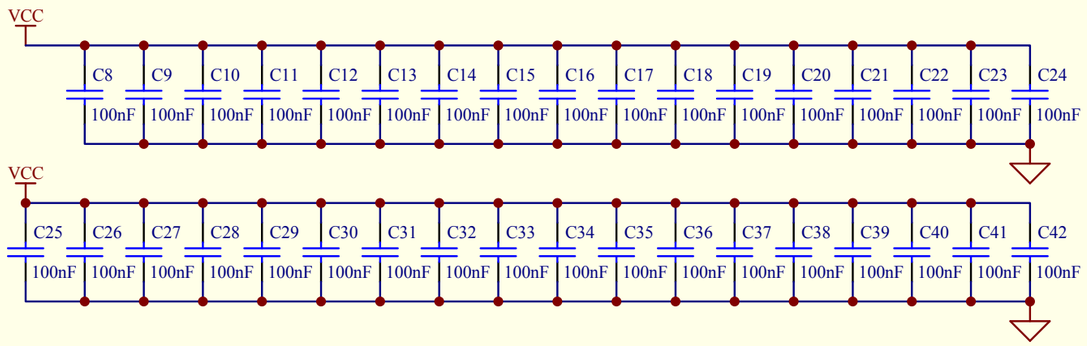


RS232 Driver

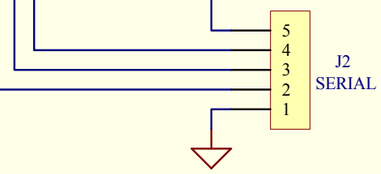


Power & Decoupling





SERIAL



Title: TTL Terminal, CPU & Keyboard		
Size: A4	Number:	Revision: V1.2
Date: 13-Mar-2023	Sheet of	
File: C:\PCBs\Computing\TTL_Terminal\TTL_Terminal_V1.2.ddb	Drawn By:	